Cleaning Options for Copper/Ultralow-k Structures

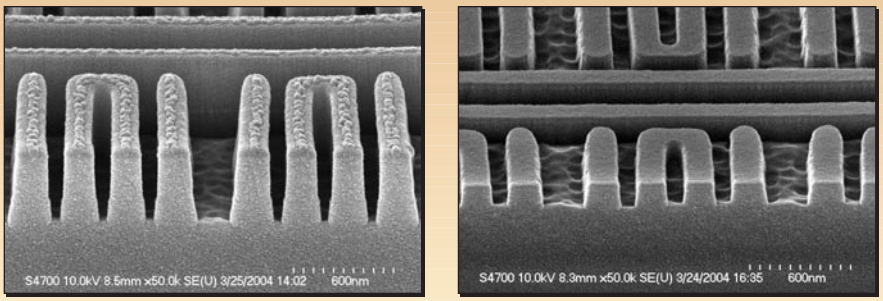
C.P.S. Hsu, B. Cruz, S. Lippy, J. Stewart, W. Cady and J. Covington,
J.T.Baker Microelectronics, Mallinckrodt Baker Inc., Phillipsburg, N.J.,
www.mallbaker.com

With the ever-shrinking dimensions of nanoelectronic devices, copper and low-k materials have been successfully integrated to produce viable products on 300 mm wafers. However, these changes have brought a host of challenges, including significant manufacturing yield issues at 90 and 65 nm geometries. As production processes move down to the 45 nm node and beyond, the need to preserve copper/low-k and copper/ultralow-k advantages becomes even more critical.

Various wafer-cleaning chemistries and technologies have been developed to work in 90 nm and below processes. Many developments have been in wet and supercritical cleans. End users can realize the highest yields by conducting a thorough analysis of methods and practices available to develop reliable and robust wafer-cleaning solutions for copper and ultralow-k integration.

At a Glance

The shift from copper/low-k to copper/ultralow-k dielectric stacks has led to a need for cleaning chemistries that preserve and restore k value. Successful cleans have been demonstrated, including one-step removal of ash residues/sacrificial ARC.



An untreated copper/low-k structure (left) and post-wet clean with CLK-222 (55°C, 30 min, right) shows efficient removal of ash residues and the sacrificial antireflective coating.

Stripping and residue removal

The major cleaning technologies for photoresist (PR) stripping and etch/ash residue removal can be classified into four categories:

- Dry cleans
- Supercritical cleans
- Wet cleans
- Alternative technologies (e.g., cryogenic aerosols, laser cleans)

Dry cleans have made steady progress in removing selected homogeneous materials; unfortunately, they have difficulties in cleaning inhomogeneous residues and removing particles. In addition, high-energy, plasma-based dry cleans generally require a hard mask to prevent excessive damage of sensitive low-k dielectrics.

Somewhat successful in etch/ash residue removal, metal ion removal and porous low-k repair, supercritical cleans require new equipment and are less efficient in bulk resist and bottom antireflective coating (BARC) removal. Their implementation into production has been delayed, as the associated costs of implementing new equipment are highly inefficient, without a guarantee of significant yield increases.

Wet cleans have advanced and delivered proven performance for processing at 90 and 65 nm nodes. They include organic-solvent-based, aqueous-based or semi-aqueous PR strippers and etch/ash residue cleaners. Integrating wet cleans with new processing tools, such as single-wafer processors, as well as mix-and-match/combining wet cleans with selected dry cleans further enhance wet cleans' capabilities. Wet and/or dry cleans are expected to perform to 32 nm and below.

Both wet and supercritical cleans are more proven and commonly used than alternative technologies, such as cryogenic aerosols and laser cleans. Generated from a precision blend of argon and nitrogen gases, cryogenic aerosols travel to the wafer surface at high velocities. In theory, the gases dislodge particles on impact, and a laminar flow field carries away the particles. Laser cleaning is designed to reduce particles from a wafer's surface without water or chemicals and with no

wetability limitations or hazardous wastes.

Preserving k value

One of the major culprits for sensitive low-k dielectric damage comes from high-energy ashing processes. Unlike the etching processes in which PRs may act as a protective layer, dry ashing of PRs and/or sacrificial ARC (SARC) with high-energy plasma frequently results in significant increases of the k value, offsetting the low-k advantages. The introduction of hard mask to protect low-k material adds process steps and increases the effective dielectric constant (k_{eff}). Chemical reactions, such as silanol capping with HMDS silylation, have been used to "repair" low-k materials;[1] however, these repaired materials do not have the identical structures and properties as the original low-k dielectrics. Alternative approaches using soft ash or reducing ash offer partial relief, but still have considerable drawbacks in maintaining low-k integrity and delivering required performances.

A number of benefits can be realized if modern wet cleans are used in copper/low-k integrations. First, modern wet cleans often use low-energy processes, limiting chemical effects/modifications at or near the surface. Also, a wide range of chemistries is available to develop suitable wet stripping/cleaning of PRs and ARCs, with minimal or virtually no damage to interconnect structures. Compatible wet-clean chemistries for ultralow-k and copper represent one of the most promising options for current and future technology generations.

Recently, enabling wet-clean chemistries have been developed. These chemistries address three key requirements of copper/ultralow-k integration:

- Stringent compatibility requirements of highly sensitive and/or porous ultralow-k dielectrics.
- Efficient removal of SARC (used for advanced lithography and patterning aid).
- Compatibility with special metal stacks in some schemes, such as copper/CoWP and copper/CoWB for reducing electromigration.[2] The commercial products cover a wide range of solvent matrices/platforms.

Successful cleans have been demonstrated in many applications, including one-step clean of bulk PR/hardened PR shell/etch residue/SARC and one-step removal of ash residues/SARC (Figure).

Processes for k Restoration (2000 Å Film, k=2.5)

Process conditions	Porous CDO capacitance (pF)	% change of dielectric constant, k (estimated)
Reference, untreated	94.4 ±0.9	—
NMP, 60°C, 30 min	124.3 ±9.7	+ (31.6 ±10)
NMP, 60°C, 30 min/RP 1*	95.8 ±2.1	+ (1.0 ±2.2)
Aqueous wet clean A, 50°C, 30 min/RP 2*	98.9 ±2.5	+ (4.8 ±2.6)
Organic solvent-based wet clean B, 60°C, 30 min/RP 3*	95.1 ±0.9	+ (0.8 ±0.9)

*RP 1, RP 2 and RP 3=Restoration protocol #1, #2 and #3 (with intermediate rinses and baking at atmospheric or reduced pressure). CDO=Carbon-doped oxide.

Restoring ultralow-k

One of the major challenges for ultralow-k integration is maintaining/restoring k_{eff} after PR stripping and residue cleans. Frequently, cleaning processes result in significant increases of k values.

Porosity often increases significantly when moving from low-k to ultralow-k materials. Unfortunately, ultralow-k materials more readily trap moisture and chemicals. Thus, cleaning processes not only are required to maintain the basic chemical and physical integrity of each dielectric, but also provide efficient ways of removing trapped moisture and chemicals.

Recent studies have shown that both selected aqueous-based and organic-solvent-based wet cleans can deliver excellent substrate compatibilities and maintain/restore the crucial k_{eff} (Table). Soaking of a porous low-k film in simple organic solvents, such as 1-methyl-2-pyrrolidinone (NMP), can considerably raise its capacitance. Various restoration protocols (RPs) are developed to restore capacitance (C; thus, k since C is proportional to k) after wet cleans. Some of these RPs could be lengthy and mainly involve alternate rinses and baking. In general, k restorations from aqueous-based wet-clean treatments are easier than restorations from organic-solvent-based chemical processes.

Supercritical cleans

The utilization of supercritical fluid ($SC-CO_2$)-based technology in wafer cleaning presents a number of advantages, including excellent mass-transfer phenomena (lack of surface tension) and enhanced ultralow-k compatibilities. Organic solvents or proprietary chemical blends are frequently used as modifiers to improve cleaning performance.

Successful back-end-of-line supercritical cleans of 90 and 65 nm wafers using both bench-top and 300 mm tools have already been conducted. Although the implementation of this new technology is expected to be further delayed, its unique properties and capabilities continue to draw interest for cleaning applications in future technology nodes.

Conclusions

Significant advances have been achieved in several areas of wafer-cleaning technologies, including wet cleans, dry cleans and supercritical fluid technology.

Coupling new chemistry developments with advanced processing tools, wet cleans show great potential to extend their proven performance to sub-65 nm generations. While delivering required substrate compatibilities, they are able to provide satisfactory cleaning of PR, hardened shell, etch/ash residues and ARCs. Furthermore, good progress has been achieved in preserving the crucial k_{eff} of sensitive, porous, low-k dielectrics. Wet cleans are expected to be able to meet the cleaning needs for 45 nm nodes and beyond. •

Acknowledgements

This subject was presented at the 22nd VLSI/ULSI Multilevel Interconnection Conf., Oct. 2005. The authors are grateful to Craig Topping and Ralph Pascoe for providing supporting experimental work.

References

1. P.G. Clark, B.D. Schwab, J.W. Butterbaugh, H.J. Martinez and P. J. Wolf, "Cleaning and Restoring k Value of Porous MSQ Films," *Semiconductor International*, August 2003, p. 46.
2. P. Singer, "Copper Challenges for the 45 nm Node," *Semiconductor International*, May 2004, p. 40.

Sherman Hsu, Ph.D., is a senior research fellow for Mallinckrodt Baker.
E-mail: sherman.hsu@tycohealthcare.com